## REMARKS

Claims 1-4, 7, 12, 13, 15, 21 and 44 are pending in this application. Claims 1-4, 7, 12, 13, 15, 21 and 44 are rejected. Reconsideration and allowance of the application are respectfully requested.

IN THE CLAIMS

Claims 1-4, 12, 13, 15, and 44 are understood to be patentable under 35 USC §103(a) over "Nassif" (U.S. Patent No. 5,963,043 to Nassif) in view of "Erickson" (U.S. Patent No. 5,970,142 to Erickson), and further in view of "Kawano" (U.S. Patent No. 6,233,339 to Kawano et al.). The rejection is respectfully traversed because the Office Action does not show that all the limitations are suggested by the references and does not provide a proper motivation for modifying the teachings of Nassif with teachings of Erickson and Kawano.

According to claim 1, a method is provided for securing communication of configuration data between a field programmable gate array (FPGA) and an external storage device. The method comprises counting a first number of oscillations of a first oscillator on the FPGA during a predetermined time interval, and counting a second number of oscillations of a second oscillator on the FPGA during the predetermined time interval. A ratio between the first number and second number of oscillations is generated as a fingerprint that represents an inherent manufacturing process characteristic unique to the FPGA. Encrypted configuration data is input to the FPGA and is decrypted in the FPGA using the fingerprint as a decryption key to extract the configuration data. None of the references alone or in combination suggests using the ratio of two oscillator counts in "generating ... a fingerprint that represents an inherent manufacturing process characteristic unique to the FPGA ... and decrypting the encrypted configuration data in the FPGA using the fingerprint as a decryption key to extract the configuration data."

Nassif's counting of oscillations of two oscillators is unrelated to any use of the counts in association with use as a decryption key, and there is no apparent suggestion or motivation for using Nassif's in generating a decryption key. Erickson's

decryptor on a PLD neither uses nor suggests the use of an inherent manufacturing characteristic of the PLD as the decryption key. Kawano's use of a sealed, fluid-filled cell in generating a decryption key does not rely on any inherent manufacturing characteristic unique to the IC, and Kawano's teachings are inappropriate for modifying Nassif.

Nassif's teachings in regards to counting the oscillations of two oscillators are unrelated to the claimed invention. Nassif teaches a method and apparatus for characterizing parasitic capacitance between IC interconnects using the ratio of pulse counts of at least two oscillators (col. 4, lines 42-57). The capacitance of the interconnects may be useful for determining the performance of the circuit (col. 1, lines 15-20). Thus, there is no apparent or suggested relevance to using the counts of the oscillators or capacitance ratio in generating a decryption key.

Erickson teaches a PLD having decryption circuit for decrypting input, encrypted configuration data ((FIG. 1; Abstract). There is no apparent suggestion by Erickson of a "fingerprint that represents an inherent manufacturing process characteristic unique to the FPGA." The cited section of Erickson teaches:

> The encryption circuit 125 then uses the key 180 to generate the encrypted configuration data 135 from the configuration data 130. The storage device 120 transmits the encrypted configuration data 135 to the decryption circuit 115. The decryption circuit 115 uses the key 180 from the security initialization circuit 114 to decrypt the encrypted configuration data 135 to generate the configuration data 130. (col. 3, lines 32-39).

There is no apparent reference in this text of an inherent manufacturing process characteristic. Applicant respectfully requests an explanation of how the Examiner interprets Erickson's text as suggesting these limitations if the rejection is maintained.

The Examiner asserts that Kawano teaches "using the ratio of the capacitance for forming a specific code for the purpose of encryption/decryption (see column 19, lines 30-50 and column 26, lines 30-41)." However, even in col. 19 where Kawano detects the static capacitance of two selected electrodes, this is not suggestive of an inherent manufacturing characteristic of the FPGA. Kawano's use of a sealed, fluid-filled cell in generating a decryption key does not rely on any inherent manufacturing characteristic unique to an IC that is to be programmed with configuration data.

Rather Kawano's cryptographic processing unit having the fluid-filled cell is bonded to a substrate along with a microprocessor and memory, for example (FIG. 1). Thus, Kawano's cryptographic processing unit having the fluid-filled cell creates the decryption key based on its own characteristics, not the characteristics of either the substrate or of the microprocessor or of the memory (FIG. 1; col. 7, lines 33-64). Furthermore, even if Kawano's cryptographic processing unit were construed to correspond to an IC with an inherent manufacturing characteristic, then the IC could not be an FPGA because Kawano's teachings are specifically directed to a fluid-filled cell with functions of the cryptographic processing unit, not those of an FPGA; Kawano's fluid-filled cell with functions of the cryptographic processing unit is not programmed with configuration data.

The asserted motivations for modifying Nassif with Erickson and Kawano are improper and unsupported by evidence. The Office Action asserts that "it would have been obvious ... to implement the features as taught by Kawano et al of using the ratio of the capacitance as a fingerprint or key for the purpose of protecting secret data against intrusion (see column 1, lines 5-12) to modify Nassif and use the ratio of the oscillations as a fingerprint or key ... to protect secret data against intrusion." However, Nassif has no apparent need to protect secret data because Nassif is directed to a test structure that is used to characterize dimensions and parasitic capacitance (Abstract). Furthermore, the Examiner has not presented any evidence that indicates what data Nassif would need to protect. Thus, even if the ratio of Nassif's two oscillation periods is proportional to the ratio of capacitance and Kawano suggests using the capacitance of two electrodes as a decryption key, there is no benefit to be gained by Nassif or reason to change Nassif's approach for characterizing dimensions and parasitic capacitance into a very different apparatus for protecting data. The asserted motivation appears to be based on a hindsight reconstruction of the present invention using the claim as a template to loosely gather elements from the prior art.

Independent claim 12 includes limitations similar to those of claim 1 as discussed above, and claims 2-4, 13, 15, and 44 depend from the independent claims.

Therefore, the limitations of these claims are not shown to be suggested for at least the reasons set forth above.

The rejection of claims 1-4, 12, 13, 15, and 44 should be withdrawn because a *prima facie* case of obviousness has not been established.

Claims 7 and 21 are thought to be patentable under 35 U.S.C. § 103(a) over the Nassif-Erickson-Kawano combination further in view of "Conn" (U.S. Patent No. 6,005,829 to Conn). The rejection is respectfully traversed because the Office Action does not show that all the limitations are suggested by the references, and does not provide a proper motivation for modifying the teachings of Nassif with teachings of Erickson, Kawano and Conn.

Claim 7 depends from claim 1 and claim 21 depends from claim 12. Thus, the limitations are not shown to be suggested for at least the reasons set forth above for the independent claims, and the asserted motivation for combining the references is improper. Therefore, the rejection of claims 7 and 21 should be withdrawn because a *prima facie* case of obviousness has not been established.

OTHER PROSECUTION MATTERS

Applicant filed an Information Disclosure Statement in accordance with 37 CFR §1.97. A copy of that statement was mailed to the Office on March 14, 2006. Applicant requests clarification as to the status of the statement and requests a copy initialed by the Examiner.

## CONCLUSION

Reconsideration and a notice of allowance are respectfully requested in view of the Amendments and Remarks presented above. If the Examiner has any questions or concerns, a telephone call to the undersigned is invited.

Respectfully submitted,

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*I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, On November 15, 2007.*

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